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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,549	04/02/2001	Yoshimitsu Nakashima	70840-55652	9425

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EXAMINER
HARRINGTON, ALICIA M

ART UNIT	PAPER NUMBER
2873	

DATE MAILED: 06/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/824,549	Applicant(s) NAKASHIMA, YOSHIMITSU	
	Examiner Alicia M Harrington	Art Unit 2873	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/02/01* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

Figures 5A-5B and 6A-6F should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants admitted prior art (figure 5A-5B pages 2-7) in view of Park et al (GB 2307344A).

Regarding claim 1, applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14); a light reception section (12); passivation section (15) film overlying the light shield section, light reception sections and aperture. However, applicant admitted prior art fails to discloses a planar /flat top surface. Although, it is well known in the art, as taught by Park et al.

In the same field of endeavor, Park discloses the planarization of semiconductor device where the passivation layer 19 is planarized (page 7, lines 22-25) Thus, it would have been

obvious to one of ordinary skill in the art at the time the invention was made to modify, applicant's admitted prior art, as taught by Park et al. to provide superior insulating property.

Regarding claim 2, applicant discloses the passivation film is made of silicon nitride based film (see pages 2-4).

Regarding claim 3-4, applicant admitted prior art fails to disclose an embodiment where an insulating film is between the passivation and light shield layer. However, passivation films that comprise several layers are notoriously well known in the art, and the Examiner takes official notice to this fact (and can comprise an insulation layer/silicon nitride layer). Further, Park discloses a BSG and insulation layer of silicon dioxide (17) directly underneath the passivation layer and over the gate layer. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify applicants admitted prior art to include an insulation layer between the passivation layer and light-shielding surface, to provide good insulation for semiconductor circuitry.

Regarding claim 5, applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14); a light reception section (12); passivation section (15) film overlying the light shield section, light reception sections and aperture. However, applicant admitted prior art fails to discloses a planar /flat top surface and chemical machine polishing as claimed. Although, it is well known in the art, as taught by Park et al.

In the same field of endeavor, Park discloses the planarization of semiconductor device where the passivation layer 19 is planarized (page 7, lines 22-25) Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify, applicant's admitted prior art, as taught by Park et al. to provide superior insulating property.

In addition, application discloses applying the thin film forming the passivation section by using a CVD technique or the like. Park uses an LPCVD process for planarization of the passivation film. Although, applicant and Park fail to produce a planarized layer using chemical mechanical polishing, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify applicant and park, to include this process since it is a notoriously well known semiconductor layering process (the Examiner takes official notice to that fact).

Regarding claim 7, applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14); a light reception section (12); passivation section (15) film overlying the light shield section, light reception sections and aperture. However, applicant admitted prior art fails to disclose a planar /flat top surface, an insulation layer and chemical machine polishing as claimed. Although, it is well known in the art, as taught by Park et al.

In the same field of endeavor, Park discloses the planarization of semiconductor device where the passivation layer 19 is planarized (page 7, lines 22-25). Passivation films that comprise several layers are notoriously well known in the art, and the Examiner takes official notice to this fact (and can comprise an insulation layer/silicon nitride layer). Further, Park discloses a BSG and insulation layer of silicon dioxide (17) directly underneath the passivation layer and over the gate layer. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify, applicant's admitted prior art, as taught by Park et al. to provide superior insulating property.

In addition, application discloses applying the thin film forming the passivation section by using a CVD technique or the like. Park uses an LPCVD process for planarization of the

passivation film. Although, applicant and Park fail to produce a planarized layer using chemical mechanical polishing, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify applicant and park, to include this process since it is a notoriously well known semiconductor layering process (the Examiner takes official notice to that fact).

Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants admitted prior art (figure 5A- pages 2-7) in view of Malazgirt et al (US 4,986,878).

Regarding claim 6, applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14); a light reception section (12); passivation section (15) film overlying the light shield section, light reception sections and aperture. However, applicant admitted prior art fails to discloses a planar /flat top surface. Although, it is well known in the art, as taught by Malazgirt.

In the same field of endeavor, Malazgirt discloses a method for manufacturing integrated circuits where the passivation film is planarized (col. 4, lines 57-65) and where in the method comprises a forming a thing film used for forming the passivation section, applying an SOG film to the thin film and performing an etch back technique (col. 3, lines 36-56). In a further embodiment, Malazgirt disclose the etch back technique is implemented such that a selective ratio for forming the passivation section is 1 to 1. (See col. 8, lines 65-68 and col. 9, line 1). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify applicant's admitted prior art, as taught by Malazgirt, since it would provide a

planarized passivation layer and circuit which is protected from ambient conditions and handling.

Regarding claim 8, applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14); a light reception section (12); passivation section (15) film overlying the light shield section, light reception sections and aperture. However, applicant admitted prior art fails to discloses a planar /flat top surface, chemical machine polishing and insulation section. Although, it is well known in the art, as taught by Malazgirt.

In the same field of endeavor, Malazgirt discloses a method for manufacturing integrated circuits where the passivation film is planarized and where in the method comprises applying an SOG film and a forming another film over the SOG for forming the passivation section (col. 3, lines 10-30) to produce a substantial planarized surface. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify applicant's admitted prior art, as taught by Malazgirt, since it would provide a planarized passivation layer which contributes to protection of the circuit and performance.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fan et al (US 6,274,917) discloses a high efficiency color filter process for semiconductor array;

Ryu et al (US 5,908,672) discloses a method and apparatus for depositing a planarized passivation layer; and

De Santi et al. (EP 0887847 A1) discloses a process for final passivation of integrated circuit devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alicia M Harrington whose telephone number is 703 308 9295. The examiner can normally be reached on Monday - Thursday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on 703 308 4883. The fax phone numbers for the organization where this application or proceeding is assigned are 703 308 7724 for regular communications and 703 308 7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 0956.

Alicia M Harrington
Examiner
Art Unit 2873

AMH
June 25, 2002

Georgia Epps
Supervisory Patent Examiner
Technology Center 2800